REMARKS

After entry of this amendment, claims 1-12 and 18-27 remain pending in the application. In the present Office Action, claims 1-22 were rejected under the judicially created doctrine of obviousness-type double patenting over U.S. Patent 6,976,194 ("Prior Patent"). Claims 13-17 were rejected under 35 U.S.C. § 101. Claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Iizuka, U.S. Patent No. 5,790,715 ("Iizuka"). Applicant respectfully traverses these rejections and requests reconsideration.

Double Patenting Rejection:

Applicant respectfully submits that the obviousness-type double patenting rejection is not supported. The Office Action asserts that the Prior Patent anticipates claims 1-22. However, the standard for anticipation is one of strict identity. While certain components of, e.g., claim 1 of the prior patent and claim 1 of the present application have the same name, the features recited for the components are not identical and thus claim 1 of the prior patent does NOT anticipate claim 1 of the present application. Claim 1 of the prior patent recites:

> A memory controller comprising: a check bit encoder circuit coupled to receive a data block to be written to memory, the memory comprising a plurality of memory devices arranged on a plurality of memory modules, each of the plurality of memory modules includes a plurality of the plurality of memory devices, wherein the check bit encoder circuit is configured to encode the data block with a plurality of check bits to generate an encoded data block, wherein the plurality of check bits are defined to provide at least detection of a failure of one of the plurality of memory modules, and wherein the plurality of check bits are further defined to provide probabilistic correction of the failure of one of the plurality of memory modules; and a check/correct circuit coupled to receive the encoded data block from the memory, wherein the check/correct circuit is configured to detect the failure of one of the plurality of memory modules responsive to decoding the encoded data block and to correct the data for the failure.

Claim 1 of the present application recites:

> An apparatus comprising:

a check bit encoder circuit coupled to receive a data block, wherein the check bit encoder circuit is configured to generate a corresponding encoded data block comprising the data block, a first plurality of check bits, and a second plurality of check bits; and

a check/correct circuit coupled to receive an encoded data block, the check/correct circuit configured to detect an error in data from one of a plurality of components and correct the error using the first plurality of check bits, the second plurality of check bits, and the data block within the encoded data block;

wherein the encoded data block is logically arranged as an array of R rows and N columns, wherein R and N are positive integers, and wherein each of the N columns comprises data bits from a respective one of the plurality of components, and wherein the first plurality of check bits form a first column of the array, and wherein each of the first plurality of check bits covers a row of the array, and wherein the second plurality of check bits form a second column of the array and are defined to cover bits in the array according to a plurality of check vectors, each of the plurality of check vectors corresponding to a different bit in the array, and each of the plurality of check vectors is an element of a Galois Field ($GF(2^R)$), and wherein the plurality of check vectors are derived from a plurality of unique elements of $GF(2^R)$, each of the plurality of unique elements corresponding to a different column of the array, and wherein the check vector in row X of the column is the product, in $GF(2^R)$ of the unique element for that column and $alpha^X$, wherein alpha is a primitive element of $GF(2^R)$.

Thus, for example, claim 1 of the Prior Patent fails to teach or suggest at least the features recited in the third paragraph of claim 1 of the present application. For at least the above stated reasons, Applicant submits that the double patenting rejection is erroneous and requests that the rejection be rescinded.

Section 101 Rejection:

The Office Action rejected claims 13-17 under 35 U.S.C. § 101. Claims 13-17 have been cancelled, and thus Applicant submits that the rejection is moot.

Section 102(b) Rejection:

Applicant respectfully submits that each of claims 1-12 and 18-27 recite

combinations of features not taught or suggested in the cited art. The Office Action alleges that the features of claims 1-22 are anticipated by Iizuka. However, the Office Action fails to actually treat all of the features of all of the claims. The entirety of the section 102 rejection is one vague paragraph which purports to cover all 22 claims. Applicant respectfully requests a full examination of all pending claims, with explicit examination of each and every feature of each and every claim.

Applicant respectfully submits that numerous features of the claims are not taught or suggested by Iizuka. For example, claim 1 recites a combination of features including: "each of the N columns comprises data bits from a respective one of the plurality of components [where the check/correct circuit is configured to detect an error in data from one of the components using the first plurality of check bits, the second plurality of check bits, and the data block, from the second paragraph of claim 1]". Iizuka appears to have no concept of a plurality of components from which a check/correct circuit receives data. Rather, Iizuka has an image sensor that reads a mesh pattern image from a recording medium (e.g. a piece of paper) and provides data that represents the mesh pattern. See Iizuka abstract. Furthermore, there is nothing to suggest that the columns of data in Iizuka's image have any correlation to components. Instead, the data is spatially ordered in the same fashion as the image, with one bit per matrix entry. See Iizuka Fig. 24, step 20-1 and the corresponding teachings at col. 23, lines 15-31. In step 20-2, the matrix is arranged as byte-sized symbols, and then the error checking codes are added in step 20-3. The array is then scrambled and various other manipulations are performed in steps 20-4 to 20-7. At no time is there any relationship of the data bits in a column and one of a plurality of components, as recited in claim 1.

Note that the error checking codes are added as follows "four checking symbols p are added to each flow (line) of the symbol matrix 400 of the target data, and four checking symbols q are added to each of 12 columns of a two-dimensional matrix formed by the symbols p" (Iizuka, col. 23, lines 54-57). Thus, every row and every column of Iizuka comprises a combination of data symbols and checking symbols. Thus, Iizuka fails to teach or suggest "wherein the first plurality of check bits form a first column of

the array" and further fails to teach or suggest "the second plurality of check bits form a second column of the array" as recited in claim 1.

Furthermore, while Iizuka teaches alpha as a primitive element in $GF(2^8)$ and using various powers of alpha to generate checking symbols, none of this teaches or suggests "the second plurality of check bits ... are defined to cover bits in the array according to a plurality of check vectors, each of the plurality of check vectors corresponding to a different bit in the array, and each of the plurality of check vectors is an element of a Galois Field ($GF(2^R)$), and wherein the plurality of check vectors are derived from a plurality of unique elements of $GF(2^R)$, each of the plurality of unique elements corresponding to a different column of the array, and wherein the check vector in row X of the column is the product, in $GF(2^R)$ of the unique element for that column and $alpha^X$".

For at least the above stated reasons, Applicant respectfully submits that claim 1 is patentable over the cited art. Claims 18 and 23 each recite combinations of features including features similar to those highlighted above with regard to claim 1, thus are each patentable over the cited art. Claims 2-12, dependent from claim 1, claims 19-22, dependent from claim 18, and claims 24-27, dependent from claim 23, are similarly patentable for at least the above stated reasons as well. Each of claims 2-12, 19-22, and 24-27 recite additional combinations of features not taught or suggested in the cited art.

Information Disclosure Statement (IDS):

Applicant did not receive the first page of the PTO-1449 form from the April 9, 2004 IDS with the present Office Action. Applicant attaches hereto a copy of the missing PTO-1449 page, along with a copy of the date-stamped postcard evidencing receipt of the IDS in the USPTO on April 12, 2004. Applicant respectfully requests that the Examiner consider the references listed on the attached page and return the initialed and signed PTO-1449 form with the next action.

CONCLUSION

Applicant submits that the application is in condition for allowance, and notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicant(s) hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-67300/LJM.

Also enclosed herewith are the following items:

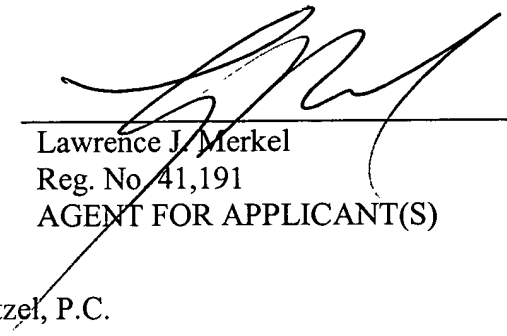
☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☒ Other: Previously submitted PTO-1449 forma and copy of date-stamped postcard evidencing receipt thereof in USPTO.

Respectfully submitted,



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